ESD: THE PROBLEMS IT CAUSES IN ELECTRONICS

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1. INTRODUCTION

It is now widely accepted that Electrostatic Discharge (ESD) events are a significant cause of device failure and that instituting static control measures is not only desirable but essential. The exact cost of ESD induced failures to the Electronics Industry is difficult to calculate since many of the costs cannot be quantified, e. g. loss of customer confidence as a result of early product failures in the field. However, it has been shown[1] that while the cost of static control measures can be high, nevertheless if correctly applied, the return on investment does justify the implementation of such measures.

MOS devices are generally regarded as the most prone to ESD damage but, in fact, all devices and technologies are susceptible, differing only in the degree of sensitivity. Furthermore, it is important to remember that ESD damage can occur at any stage from device production through system assembly, testing and packaging to final use in the field.

2. THE ORIGIN OF THE PROBLEM

ESD problems have arisen in the last decade because of two major developments.

(a) The increasing use of man-made fibre and plastics in clothing, soft furnishings and furniture has led to an increasing propensity to static charge generation on the factory floor, in the office and in the home particularly where air conditioning reduces the ambient relative humidity.

(b) As complexity increases, it is necessary to fabricate integrated circuits from smaller and smaller device elements in order to achieve higher operating speeds and improved production yields.

The intrinsic electrical properties of man-made fibre and plastic materials are such as to render them very good insulators, their bulk resistivities exceeding $10^{14}\Omega$m. When brought into contact with other insulating, or even conducting materials they will become electrically charged by a process known as triboelectrification. Such charging cannot be prevented since it is a natural consequence of electron (or possibly ion) transfer between two contacting surfaces[2], a process which brings the surfaces into thermodynamic equilibrium. As a result of the charge transfer, one surface acquires a positive charge and the other a negative charge. The degree of charging depends on (i) the intimacy of the contact, (ii) whether any rubbing occurs during contact and (iii) the manner in which the surfaces are separated. Generally, the

highest charge levels are generated when surfaces are rubbed rapidly together under high contact pressure and then separated quickly from each other so as to minimise the opportunity for the transferred charges to recombine. Once generated, static charge can remain on the surface of good insulators for minutes, hours and even days unless steps are taken to neutralise it. Electrically isolated metal surfaces can also retain static charge thereby posing an ESD threat.

In the workplace, static can be generated on benchtops, on furnishings, on carpets as well as on the devices themselves. The major problems, however, arises from static generated on personnel as they carry out their normal day-to-day tasks. Results have been published [3] of several surveys in which the static charge generated by various operations has been measured. These have shown that voltages as high as 15kV may be generated on personnel walking on carpets and that 5kV may be developed simply by rising from a PVC covered chair. Removing devices and circuit boards from certain types of plastic bubble packs can generate equally large voltages.

An electrostatic discharge occurs from any charged object if the electric fields associated with the charge exceeds the electrical breakdown strength of air (~3 MV/m). The breakdown results in a rapid release of the electrical energy stored on the charged object. Where discharges occur from personnel to the pins of a device, the duration of the discharge may well be much less than a microsecond, and during the discharge, currents in excess of tens of Amperes may flow.
The susceptibility of devices to ESD arises primarily from the ability of present day technology to define features no more than a few microns in size. This means that currents within a device are constrained to flow along well-defined paths of very small cross-sectional area. About 5μJ of energy is sufficient to blow a 5μm diameter crater in silicon. Compare this with the human body which has a capacitance of about 150pF and when charged to 5KV has 1.9mJ of stored electrical energy. During an ESD event from such a person, sufficient current will flow through junctions or interconnecting metal or polysilicon conductors to cause local.. melting or even vapourisation[3]. Device elements thermally isolated from the semiconductor substrate are the most likely to suffer damage since heat dissipation from these elements is restricted. Thus interconnects placed on thick oxide or nitride layers will be vulnerable and the emerging silicon-on-insulator technologies will be particularly sensitive to this type of damage.

The high sensitivity of MOS technology to ESD events arises primarily from the very thin gate insulation employed. The electrical breakdown field of thin silicon dioxide layers is 8 x lO^8V/m and since a typical gate oxide thickness may be as low as 20 nm, voltages greater than 16 V appearing on the gate terminal will be sufficient to cause electrical failure of the layer. The importance of ensuring that such devices are not exposed to high static potentials is obvious.

Within the next decade, submicron devices will come into general production, so that the sensitivity of individual device elements to ESD events will be greatly increased. Therefore, protection against static charge damage will of necessity be an evolving processing and each new production change will have to be audited to ensure that it does not introduce additional static-related problems.

Although electrical discharges direct from personnel to the pins of a device probably account for most static-related damage, other failure modes are possible. For example, the pins of a

DIL package may acquire a tribocharge when sliding out of its shipping tube. The charge is likely to be distributed on the metal interconnects and because of the capacitance associated with the device, high voltages may appear on the pins. When the device is inserted into a board, the stored charge is rapidly dissipated causing damage similar to that from charged personnel.
Insertion of devices into circuit boards is often carried out automatically thus reducing significantly the risk of personnel related ESD events-during manufacture. However, care is necessary to ensure that the equipment used cannot expose the device to damaging levels of static. This will become more important as production speeds inevitably are increased. Static dissipative materials that are effective at low production speeds may well give rise to static problems at higher throughput. Similar. care is necessary when devices are checked in automatic testers.
Static related damage may also occur when charged objects e.g. plastic packaging, personnel or plastic tools move rapidly in the vicinity of a device. Coulombic forces of attraction and repulsion will induce a redistribution of charges within the device, causing currents to flow through interconnects and voltage transients to occur between adjacent circuit elements. These currents and voltages may be sufficiently large to cause damage and since they are induced within the device, measures taken to protect the input pins would not, in general, be effective in protecting the device.

3. LATENT DAMAGE

Total failure of a device during production will usually be noticed during routine testing of the device itself or the board on which the device is mounted. Such losses, while inconvenient, are not particularly costly. Amore troublesome and potentially more costly problem is 'Latent Damage [4] which is a subcritical form of damage introduced during production. Devices suffering from latent damage appear to be within specification when tested but are prone to early failure in the field.

Latent damage occurs when the energy of an ESD event is below the critical level required to produce total failure. For example, an interconnect may only partially erode during the ESD event. However, when the device is in continuous operation, local Joule heating may cause further erosion at the same location eventually leading to an open circuit. It has also been shown that when large current pulses from ESD events pass through metal-semiconductor contacts, Joule heating may be sufficient to cause local alloying of the aluminium and silicon leading to the formation of 'alloy spikes' which can propagate either vertically or laterally from the contact pad. eventually short-circuiting nearby junctions. The corners of diffusion wells s are very prone to latent damage because of the field enhancement that occurs there.

4. SENSITIVITY OF ELECTRONIC SYSTEMS

It is tempting to believe that once a device has been mounted onto a circuit board it is safe from ESD damage. On the contrary, it may well be more vulnerable since the pins may be connected to long, isolated conductors which may become charged when handled by personnel e. g. during removal from plastic packaging.
Complete systems are also vulnerable especially when enclosed in an insulating plastic case since discharges from a plastic case may corrupt the system memory. Charged personnel

moving in the vicinity of the system may induce significant current flows in the system. Recent experiments [6] have shown that threshold levels for ESD-induced latch-up of a desk top computer depended sensitively on the screening and earthing arrangements adopted. Although earthed, conducting screens must improve immunity to electromagnetic interference, it is also suggested[6] that a less conductive, though not insulating, enclosure may be advantageous in ESD protection by dissipating static charge more slowly, thus avoiding large current flows in the screen.

5. AVOIDING THE PROBLEM

Protection at the device level can be built-in by the device manufacturer. This is usually achieved by including at each pin a fast acting diode or transistor switch to divert the discharge current away from the sensitive node through a dissipating resistor[7]. Using these techniques, it is possible to reduce significantly the sensitivity of devices to ESD events [8]. However, these protection circuits will reduce the frequency response of the device. Furthermore, the device may be exposed to a very energetic discharge which damages the protection circuit so that the device becomes vulnerable again.

Good circuit layout can also help to reduce the problem. In addition to optimising the layout so that the device meets its performance specification, the device designer should also consider the problems posed by electric field enhancement at the corners of diffusion wells and interconnects, particularly where device elements are located close to each other. Much evidence has been presented which indicates that such areas are the most vulnerable to the ESD event.

Although some on-board protection is provided on modern devices, the degree of protection afforded is variable. The onus is very definitely on the device user to adopt sufficient precautions to ensure that the device is not exposed to damaging levels of static electricity. Indeed, even a few relatively simple countermeasures can be beneficial. Advice is readily available in the form of Standards e. g. DOD-STD-1696 or BS 5783: 1984 and 1987, and as papers presented in Conferences on ESD/EOS. However, most large companies have developed their own in-house procedures and are happy to share their experience and knowledge with their customers.

Ideally a Special Handling Area (SHA) should be established in which sensitive operations are performed. Within the SHA, all personnel must be correctly earthed with wrist straps and should wear appropriate clothing. All benchtops, furniture and flooring materials should be capable of dissipating static electricity to earth within a very short time, say lms of it being generated. The relative humidity should be controlled so that it never falls below 30%. The cost of setting up and running the SHA can be large and so it is important to plan carefully and to seek expert advice[9].

Although setting up an SHA is an important step, careful auditing of all device, board and system handling procedures is necessary from Goods Inwards through to Shipment. Appropriate containers should be used to protect devices during transport between various production stations. The precautions must also extend to in-service maintenance.

Special static monitoring instrumentation should be purchased or hired for the audits and personnel trained to carry out and interpret the measurements.

Finally, and most importantly, an awareness of ESD and the problems it creates must be engendered in all personnel who handle static sensitive devices.

6. CONCLUSIONS

ESD is now recognised as a source of device damage and reduced system reliability. The mechanisms of damage in the device are being slowly identified and this is providing the circuit designer with an opportunity to improve the 'hardness' of his devices by improved circuit layout. While on-board protection reduces the sensitivity of devices to ESD, nevertheless, the main responsibility remains with the user to ensure that devices are not exposed to damaging levels of static electricity.

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